Amendments to the Claims

1. (Original) A dual gate oxide high-voltage semiconductor device, comprising:

a buried oxide layer formed over a semiconductor substrate;

a silicon layer formed over the buried oxide layer;

a top oxide layer formed over the silicon layer;

a first gate oxide formed over the silicon layer adjacent the top oxide layer; and

a second gate oxide formed over a portion of the first gate oxide.

2. (Original) The device of claim 1, wherein the silicon layer comprises a source region, a body region, and a drift region.

3. (Original) The device of claim 2, wherein the first gate oxide is formed over the drift region, the body region, and the source region.

4. (Original) The device of claim 2, wherein the second gate oxide is formed over the first gate oxide between the top oxide layer and the body region.

5. (Original) The device of claim 1, further comprising a field plate formed over the top oxide layer, the first gate oxide, and the second gate oxide.

6. (Original) The device of claim 1, wherein the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A.

7. (Original) The device of claim 1, wherein the first gate oxide has a length of approximately 3-4μm, and wherein the second gate oxide has a length of approximately 1-2μm.

8. (Original) A dual gate oxide high-voltage semiconductor device, comprising:

a buried oxide layer formed over a semiconductor substrate;

a silicon layer formed over the buried oxide layer, wherein the silicon layer comprises a source region, a body region, and a drift region;

a top oxide layer formed over the silicon layer;

a first gate oxide formed over the silicon layer adjacent the top oxide layer; and

a second gate oxide formed over a portion of the first gate oxide between the top oxide layer and the body region.

9. (Original) The device of claim 8, further comprising a field plate formed over the top oxide layer, the first gate oxide and the second gate oxide.

10. (Original) The device of claim 8, wherein the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A.

11. (Original) The device of claim 8, wherein the first gate oxide has a length of approximately 3-4μm, and wherein the second gate oxide has a length of approximately 1-2μm.

12. (Previously Amended) The device of claim 8, wherein a thickness of approximately 1200A of the second gate oxide results in an increase from approximately $1e^{12}cm^{-2}$ to approximately $2e^{12}cm^{-2}$ of a maximum allowable charge and a decrease of approximately 30% of a specific-on-resistance, of the device.

Claims 13-20 (Previously Cancelled).

21. (New) A dual gate oxide high-voltage semiconductor device, comprising:

a buried oxide layer formed over a semiconductor substrate;

a silicon layer formed over the buried oxide layer, wherein the silicon layer comprises a source region, a body region, and a drift region;

a top oxide layer formed over the silicon layer;

a first gate oxide formed over the silicon layer adjacent the top oxide layer; and

a second gate oxide formed over a portion of the first gate oxide between the top oxide layer and the body region, wherein the second gate oxide and the first gate oxide form a stepped oxide region.